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Yield Improvement of Wafer Edge Die Defocus at Lithography Process for 0.16µm CMOS Technology

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Abstract: *The lithography process is the heart of the semiconductor process. The process is to transfer the circuit design on the wafer substrate via reticle at the expansive lithography equipment. It's a critical process, where any defects if not detected caused scrap to wafers of deformity found in the pattern a possible rework with series of etching and cleaning equipment needed that easily took a day loss of cycle time in the hectic high utilization manufacturing facility. The research focuses on the new technology of 0.16µm that facing an issue of poor pattern formation at the edge of the wafer and its damage area will be the show stopper to introduce for high volume manufacturing. This research is focus to minimize the defects by optimizing the process recipe Improve Inner & Edge Die Bias (IIEDB) being explored at the Deep Ultra Violet (DUV) 193nm wavelength equipment. The recipes that combine the temperature of baking and radial exposure parameters help significantly to reduce the defect. Measurement of good die versus bad die of a wafer unit in percentage being used for an electrical and functional test that also known as sort yield is used in the paper. The new finding has shown significant results to reduce yield loss issues at the edge region and able to improve the edge die sort yield from 50% to 85% and the electrical yield from 81% to 94%. This paper will discuss the journey for edge die defocus improvement.*

Keywords: Edge Dies, Lithography, Partial Field Region, Semiconductor

1. Introduction

The semiconductor of wafer manufacturing is consisting of series of repeated process steps to build an integrated circuit (IC). An IC consists of several components of electronic devices such as a transistor, capacitor, and diode. The fabrication process of an integrated circuit (IC) comprises multiple step sequences of chemical and photographic operations done on a wafer. Most semiconductor chip makers primarily employ a wafer or substrate manufactured on a thin slice of silicon. The following stages are involved in the production of an integrated circuit: silicon wafer, epitaxial, photolithography, etching, cleaning, and doping (Snider, 2005).

The photolithography process has the most complicated, expensive equipment and critical process in the semiconductor wafer process and one of the bottleneck processes in the production line when compared to other wafer manufacturing methods. Photolithography is the process of temporarily coating a wafer with a photoresist and transferring a specified pattern to the photoresist, which is the core of the manufacturing process flow (Yen & Changt, 2012). The photolithography process aims to achieve high resolution and high photoresist sensitivity with minimal feature size, precise process control, and low defect density.

Photolithography (Pease & Chou, 2008) is the process of transferring a geometric design from a Photomask to a light-sensitive photoresist on a substrate using light. After the developing process, the photoresist must be removed. The photolithography process sequence includes photoresist coating, alignment, exposure, and photoresist development of the layer. It necessitates excellent resolution, very sensitive alignment, and low defect density, all of which lead to high yield and good imaging techniques. Photolithography is transforming complex circuit diagrams into a pattern on the wafer with successful exposure and process step to form a superimposed layer of semiconductor materials.

As the technology is shrinking, yield improvement is the major challenge in the wafer fabrication process. Product yield losses in the semiconductor manufacturing process are frequently caused by contamination involved in the fab environment, process variation, and scrapped due to defects which are significant impacts on profitability.

Edge die yield loss is the most critical issue at semiconductor manufacturing fabrication. At the Lithography process, the edge dies yield loss mechanism is caused by pattern uniformity issues at wafer edge dies, pattern distortion, pattern lifting, and defocus due to topography issues caused by incoming process-related issues.

To solve the edge dies yield loss issue, most of the IC makers have decreased wafer edge exclusions in recent years to shape semiconductor devices closer to the wafer edge (Strobl et al., 2010). While the aim is to create more excellent dies per wafer, the yield of die towards the edge is generally lower than that of die in the wafer's core, as illustrated in Figure 1.

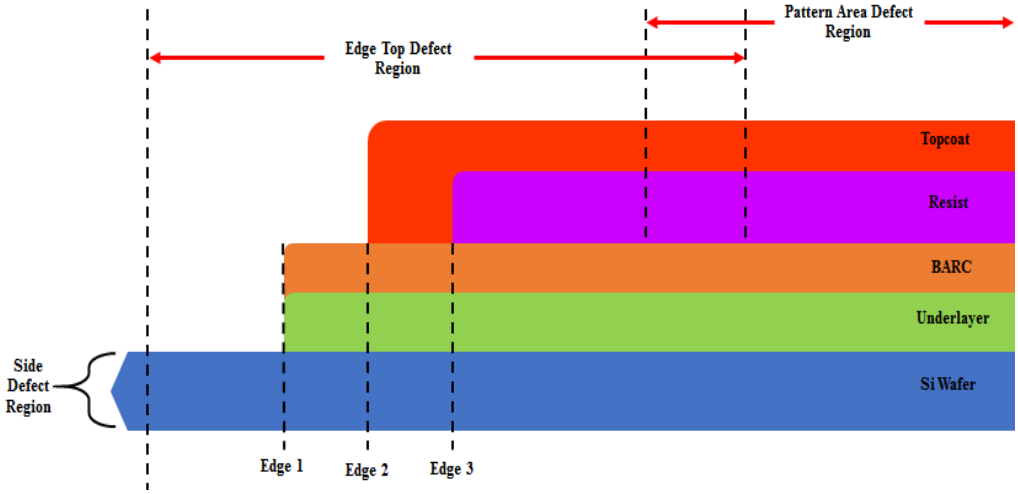

Figure 1: Lithography Wafer edge profile design from Undercoat to Topcoat

The improvement in yield at the wafer edge is a focus on productivity and cost reduction. The wafer map is divided into five areas: center, center radius, edge, and outermost edge. In wafer semiconductors, wafer edge die defocus occurs at the outermost edge 1 to edge 3 regions, as shown in Figure 1. Hence, this research focuses on the edge and the outermost edge of the wafer on the Lithography process for 0.16µm Complementary Metal-Oxide Semiconductor (CMOS) technology.

The uniformity of topography from the incoming process steps is related to the yield at the wafer edge and outermost edge of the wafers. At the Lithography process, edge bead removal (EBR) is one of the standard requirements process steps. EBR is to remove the resist on the

edge of the wafer to reduce the potential contamination and enable the vacuum chuck to hold the wafer.

Tight control of the edge trim widths of the imaging film is necessary to ensure that the films land on the desired surfaces and that the horizontal edge spacing to minimize while maintaining the designed profile. The most important parameters of the film EBR metrology are shown in Figure 2. The nominal edge widths were chosen to ensure that the topcoat film completely encapsulates the resist layer and to complete the top coat on the BARC layer to which it will adhere well.

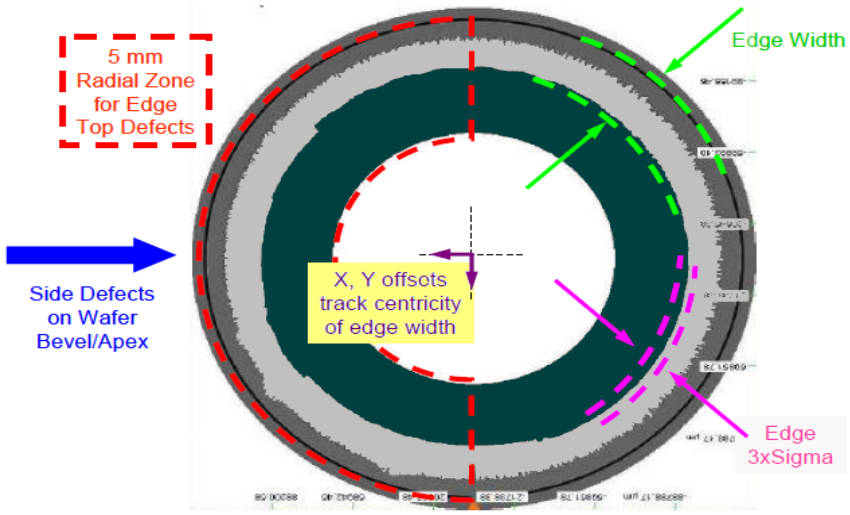

Figure 2: EBR inspection metrics relative to the second film edge (Corliss et al., 2016)

The 3-sigma value is a measure of the variability of the edge width and is determined by the accuracy of the center placement of the wafer on the coating bowl chuck and the EBR process consistency (e.g. EBR arm stability, solvent pressure stability). The X and Y offsets show any translational shift in the difference between the film edge and the wafer edge, integrated over the 360° measurements (Corliss et al., 2016). Eventually, this condition would present a significant contamination risk not only for the resist track and the exposure tool but for process equipment outside of lithography as well.

Figure 3 shows the stacking map of 388 wafers of current yield performance for 0.16µm technology products and the mean of the yield is 81.4% and towards the edge dies the yield becomes the lowest.

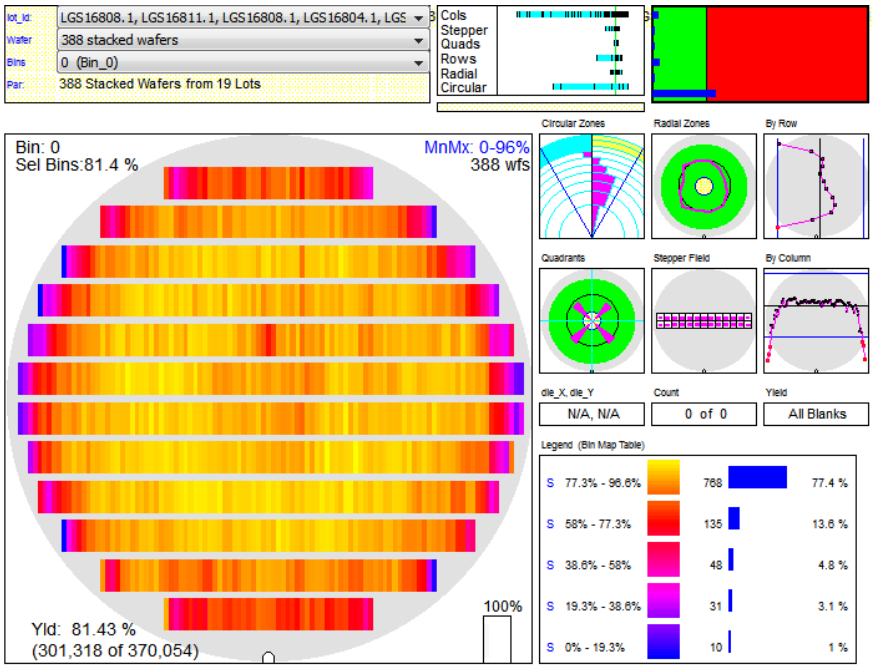

Figure 3: Stacking yield map for 0.16µm technology

Figure 4 shows the stacking map of yield data by zonal area from center to edge region and the yield at wafer edge regions is lower than compared with the center region.

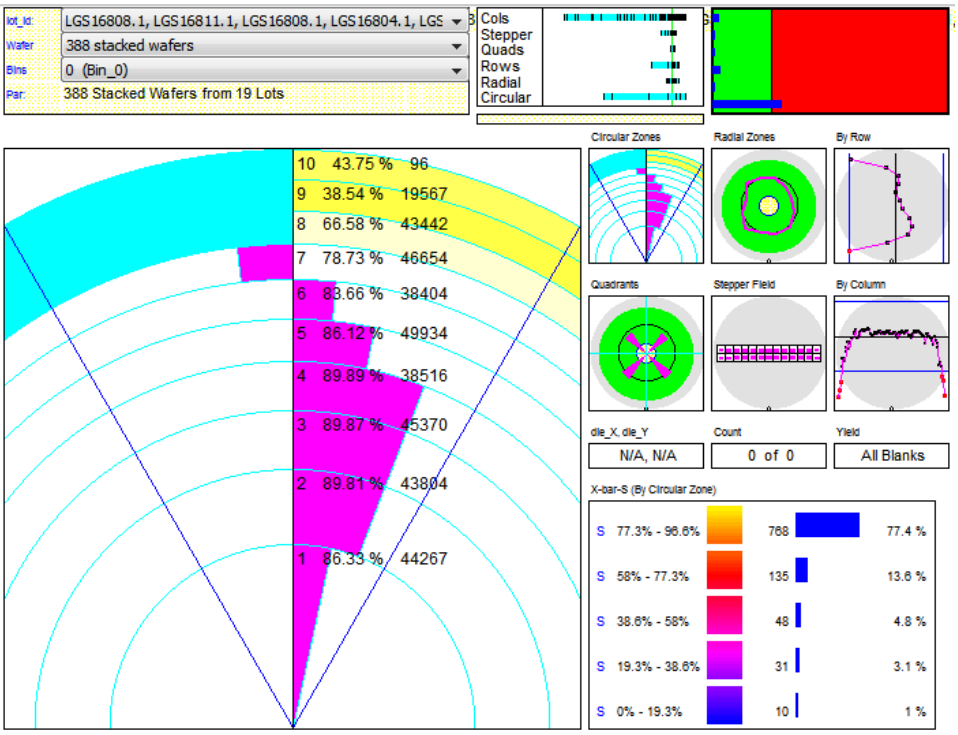

Figure 4: Stacking yield map for 0.16µm technology by zonal area

The zone is divided into a 10-zone data set that extends from zone 1 to zone 10. Zone 1 is the center of the wafer and zone 10 is at the edge of the wafer. The yield in zone 1 is 86% and in the direction of zone 10, the yield decreases in each zone. In zone 10 the yield deteriorates to 43.7%. This is due to the effect of defocusing the edge dies. The purpose of the research is

therefore to investigate the effect of defocusing the edge chip, which causes the loss of yield in the edge area of the 200 mm wafers for the 0.16µm technology.

2. Literature Review

Some literature is reviewed to provide a theoretical basis for the research in this chapter, which is structured as follows. In the first section, the term photolithography and the challenges used in this paper are clearly defined and the importance of understanding the module process photolithography (Quirk & Serda, 2002) summarized. In the second section, the problem of yield loss caused by the defocusing of the edge dies is well explained to build a framework for the analysis of the EDD problem from the various findings and causes in the later chapters. In the third section, an adapted research framework is created based on the analysis framework to compare and evaluate the EDD topic according to the research objectives.

This paper describes the wafer edge yield engineering methodology that was essential to the reported steep production. Several factors can cause significant yield losses (Delahaye et al., 2009), factors including non-uniformities in film thickness and etch profiles due to plasma inhomogeneity to the wafer edge; Wafer warpage due to film stress; Residues on the bevel and back; Feed damage from reactive gases or particles; and mechanical damage to the bevel caused by plasma or handling.

Systematic defects caused by layout patterns can be associated with diffraction effects induced by sub-wavelength lithography. As briefly explained in the introduction, diffraction-induced effects in lithography can be traced back to pattern proximity effects. Therefore, it is important to predict systematic defects due to lithography through an effective litho-based yield modeling methodology. The first part of this chapter assumes the development of such a methodology to predict the overall yield of the design based on lithography simulations. Given the effects induced by lithographic perturbations on mask features, an a-line shape model predicts the failure probability of the regions examined (Sreedhar, 2011).

Figure 5 shows the current issue at 0.16 micrometers processes. The scanning electron microscope (SEM) images show the difference between edge dies and center dies. As the edge dies shows the topography is affected by defocus and whereby the center dies formed well accordingly. The main issue of edge dies yield issue is due to the topography difference between wafer edge and center due to coating, etching, and polishing non-uniformity which is causing the edge die defocus issue. Edge die defocus can be caused by various reasons: Particles in the stage scanner, topology, adhesion of BARC, scanner edge set offset, resist bridging, resist lifting & contact / via missing.

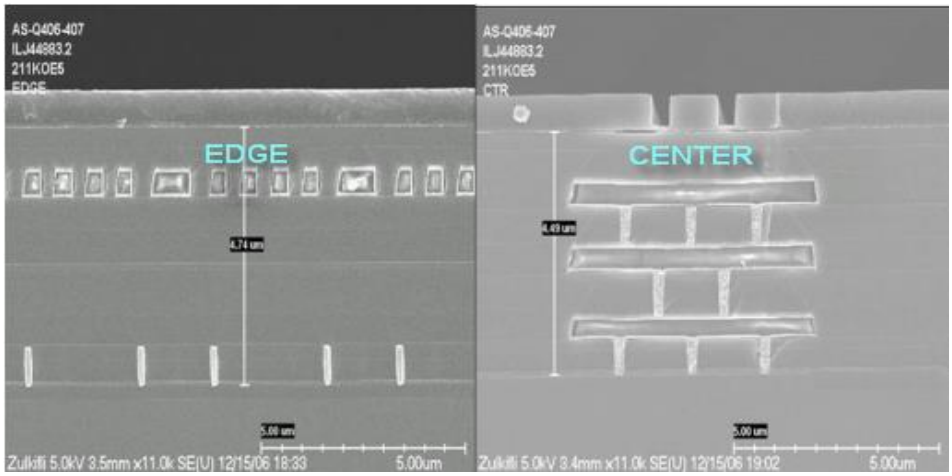

Figure 5: Electron microscope image of edge die defocus

For effective process control, semiconductor manufacturing must detect edge defect effects due to topography issues. This due to varying thickness, wafer handling, and scratches. While pre-production wafer inspection is likely to find only a handful of defects, applying the same techniques to a back-end product wafer can find hundreds or even thousands of anomalies (Burkeen et al., 2007).

According to (Huey et al., 2012; Komarenko et al., 2012), as the technology continues to shrink, tighter requirements are demanded of each of the CMP process steps involved in the integration process flow. With the introduction of the Replacement Metal Gate (RMG) process, additional CMP steps have been added that critically enable this integration scheme.

As the technology is shrinking from 500nm to 32 nm, the defectivity is increasing day by day in the IC manufacturing process. Defects from the edge die of wafers have a significant impact on yield. Defects that initiate from the edge of semiconductor wafers have a momentous impact on device yields and several good dies, which are attained from each of the wafers. To reduce the defocus at the edge dies, it is possible to minimize the marginal exclusion ring down to 1.5 millimeters. By minimizing the edge exclusion to 1.5nm, it is possible to increase the number of good dies at the edge region. Eventually by reducing the edge exclusion and minimize the impact of the yield loss at the wafer edge, however, there are high chances to loss completed died at the edge region.

There are many ways to produce better yield at the wafer edge but based on the previous research or method, there's an affecting of properties and limitation to continue with their improvement or findings. Studies on EDD had only focus on understanding the process and the aspect of Photolithography and the resist coating. However, there's very limited work has been done to investigate the Edge Die Defocus under the aspect of Photolithography. The CMP aspect study and investigation had been investigated thoroughly. However, it was believed that the limitation set accordingly with 3mm exclusion, which will minimize the number of dies in the wafers such as more than 30 good dies unlikely to lose as shown in Figure 2.30.

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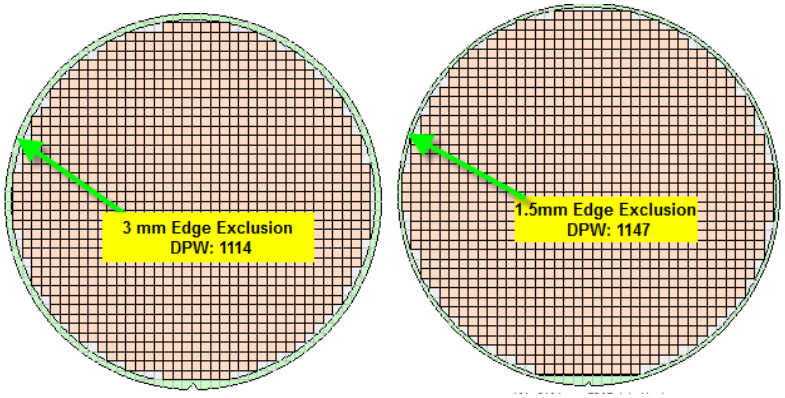

Figure 6: Electron microscope image of edge die defocus

3. Methodology

The research methodology was designed to improve the edge die yield issue at 0.16 µm technologies as having an edge die to defocus issue. Introduced six phases research methodology in this research could able to rectify the EDD issue and improve the edge die yield issue for 0.16µm technologies.

The principle substrate with POR condition thickness uses current work to continue the methodology to prove that it can improve the yield at the edge dies. Photo defects are difficult to detect on product wafers because the noise from the topography, grain, and color of the underlying layers confounds the detection of current-layer defects, as mentioned previously. In particular, many lithography defects have low topography, subtle color variation, and/or small physical extent. All of these characteristics mean that the signal for optical detection is small. Thus, reducing the denominator in the signal-to-noise ratio by removing the additional challenge of detection on a product wafer raises the capture probability of defects having these characteristics, thus every single process optimization required defect inspection to confirm that the methods are suing is free from contamination of particle or process-induced defects. In every type of defect need to be carried out different types of containment action require continuing this study.

To determine the target condition as explained in research methodology, the study will continue with POR resist with various thickness and illumination setting to verify the critical dimension (CD) bias and the defects optics, the numerical aperture (NA) of an optical system is a dimensionless number that characterizes the range of angles over which the system can accept or emit light. By incorporating the index of refraction in its definition, NA has the property that it is constant for a beam as it goes from one material to another, provided there is no optical power at the interface. The exact definition of the term varies slightly between different areas of optics. Thus, NA is commonly used in microscopy to describe the acceptance of a pattern or image.

The research methodology consists of five phases which will lead to complete the objective of this research to identify the best-known method to eliminate the edge die defocus to improve

the overall yield for 0.16µm technology. Briefly, the first phase is to identify the actual problems that occur in the project and the major factors that cause the problem. Once the major factors of the project's problem are identified, continue with the second phase and third phase evaluation with a new illumination setting. Phase fourth and five are evaluated with the new Reticle Exposure Latitude (REL) method approach.

The experimental work selected the process conditions with optimized resist thickness and parameters for coating, exposure, and development process. Once the selection is complete, it continues with the focus exposure matrix (FEM) condition to check the process window of the depth of focus (DOF). Phase 1 comprised experimental work, which will lead to complete the goal of this research of identifying the most popular method of removing edge die defocus issue to improve the overall yield for the 0.16µm technology. In addition, this experimental work will include the methodology and each step will be explained accordingly. In short, the first experimental work is done to identify the real problems that arise in the project and the main factors that are causing the problem. Once the main factors of the project problem are identified, the second experimental work and the third experimental work with a new lighting setting will be assessed. The fourth experimental work up to the sixth will be evaluated through the introduction of to improve inner and edge die bias framework.

Table 1: Experimental six essential phases in the methodology

Experiment No.	Thickness	Illumination Setting
Experiment 1	6300A	POR – Numerical Aperture 0.6
	8500A	POR – Numerical Aperture 0.6
	10200A	POR – Numerical Aperture 0.6
	13000A	POR – Numerical Aperture 0.6
Experiment 2	6300A	Numerical Aperture 0.55
	8500A	Numerical Aperture 0.55
	10200A	Numerical Aperture 0.55
	13000A	Numerical Aperture 0.55
Experiment 3	6300A	Numerical Aperture 0.65
	8500A	Numerical Aperture 0.65
	10200A	Numerical Aperture 0.65
	13000A	Numerical Aperture 0.65
Experiment 4	6300A+REL 1	NA 0.55, SOB 90c
	8500A+REL 1	NA 0.55, SOB 90c
	10200A+REL 1	NA 0.55, SOB 90c
	13000A+REL 1	NA 0.55, SOB 90c
Experiment 5	6300A+REL 2	NA 0.55, SOB 100c
	8500A+REL 2	NA 0.55, SOB 100c
	10200A+REL 2	NA 0.55, SOB 100c
	13000A+REL 3	NA 0.55, SOB 100c

The research methodology was designed to improve the edge die yield issue for 0.16 µm technologies as having an edge die to defocus issue. Introduced six phases research methodology in this research could able to rectify the EDD issue and improve the edge die yield issue for 0.16 µm technologies. At the end of the experiments, the result will conclude accordingly to improve the EDD issue with the new improvised method.

Bare silicon wafers were used for this purpose instead of stacked oxide wafers. Due to the restricted number of lots and time constraints, this experiment used three wafers at each experimental step. As per the data collection purpose and for statistical analysis purposes, three wafers data are good to compute by analysis of variance (ANOVA) to compare the within factor variance with the between factor mean variances.

The photoresist thickness 6300Å, 8500Å, 10200Å, and 13000Å is coated with a new illumination setting 0.6 µm and 0.55 µm with different temperature condition of Soft Bake (SOB) condition. After spin coating, the typical average concentration in the resist film is between 20% (thin films) and 40% (thick films), since the CD bias is the concentration of this project, SOB temperature condition is the most important parameter to validate in each experiment.

As an initial test, a focus exposure matrix (FEM) was performed to identify the process window margin. FEM condition is set as predefined setting set by device and technology-based at Lithography module process qualification method. The FEM condition is selected based on POR condition as;

- Resist thickness 6300Å
- Dose 33mJ as nominal dose and step to 1mJ
- Focus 0.1 µm as nominal focus and step 0.1 µm

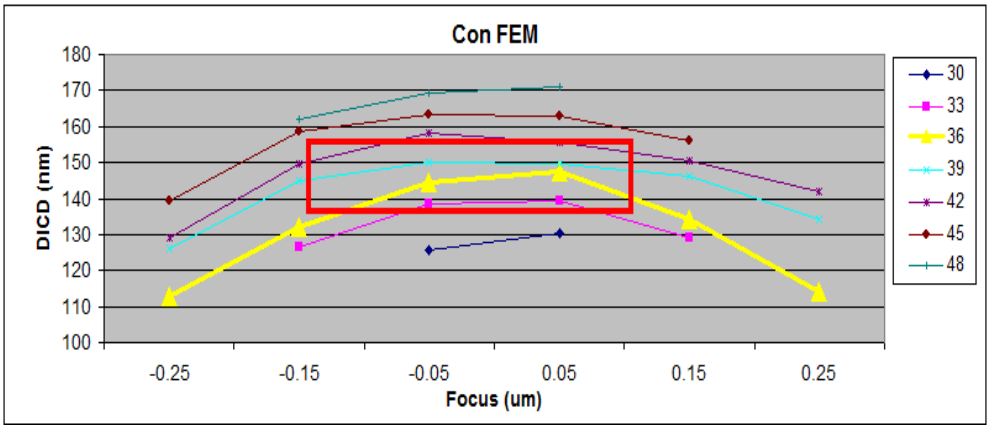

Figure 7: Electron microscope image of edge die defocus

The process window is around 0.3 µm as highlighted by the red color box. The more the process window is the best the optimum level to enhance the Litho process. The process window is to ensure greater than 0.3um to avoid any process drift or tool drift which will lead to rework or scrap the wafers due to process variation. The FEM result from the POR condition shows that if the focus is toward to negative either towards to positive side is end up with pattern collapse. Figure 8 shows the FEM images of the process window are from 0 µm to 0.2 µm with good images and towards the positive side 0.3um onward pattern is distorting. On the negative side

at –0.1 µm image is getting blur. This shows that the process window is only 0.3 µm only as highlighted with a red box.

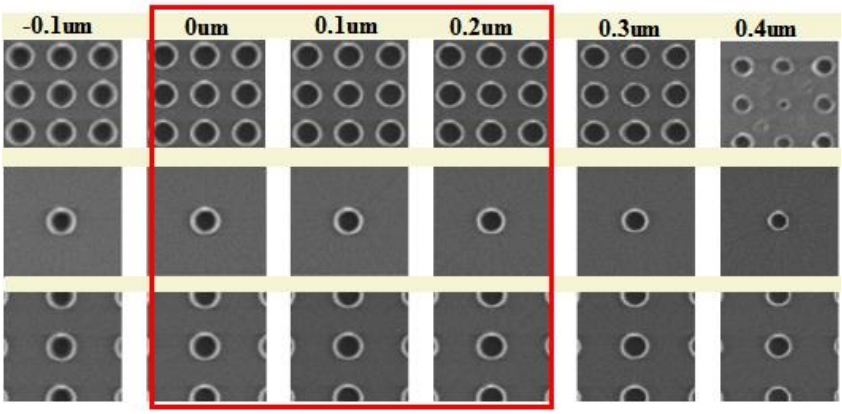

Figure 8: Electron microscope image of FEM

An experiment with the REL method is proceeding with;

- NA setting 0.55 µm as same as phase 2 setting
- Soft-Bake (SOB) temperature increased from 90 Celsius to 100 Celsius
- Applied radial exposure method and dose energy at inner dies will be 25.5mJ as nominal dose energy

This entire experiment process to identify the possible solution to eliminate the edge dies defocus issue to improve the overall wafer yield. In this research, the aim is to increase the edge die yield by reducing or eliminating the defocus issue on the wafer edge region by introducing REL Framework. In the experiment's total of five experimental conducted and all the experiments with some significant improvement to overcome the issue. From table 4.10, results show from all the experiment results from experiments 1 to 5. Experiment 1 is the POR data collection for baseline purposes. Experiments 2 to 5 with the new approached method to improve the EDD issue.

Table 2: Experimental six essential phases in the methodology

Experiment No.	Thickness	Illumination Setting	Centre to Edge Bias Cycle Test 1	Centre to Edge Bias Cycle Test 2	Centre to Edge Bias Cycle Test 3
Experiment 1	6300A	POR - Numerical Aperture 0.6	50.1nm	51.9nm	50.5nm
	8500A	POR - Numerical Aperture 0.6	51.5nm	53.4nm	52.7nm
	10200A	POR - Numerical Aperture 0.6	49.7nm	51.3nm	51.7nm
	13000A	POR - Numerical Aperture 0.6	50.4nm	51.8nm	52.3nm
Experiment 2	6300A	Numerical Aperture 0.55	39.6	36.5	33.7
	8500A	Numerical Aperture 0.55	36.6	36.5	33.7
	10200A	Numerical Aperture 0.55	35.9	36.2	35.4
	13000A	Numerical Aperture 0.55	31.7	35.3	34.8
Experiment 3	6300A	Numerical Aperture 0.65	28.5	29.7	29.4
	8500A	Numerical Aperture 0.65	26.7	27.4	26.8

	10200A	Numerical Aperture 0.65	25.4	25.7	25.8
	13000A	Numerical Aperture 0.65	27.2	24.5	29.1
Experiment 4	6300A+REL 1	NA 0.55, SOB 90c	22.7	25.6	27
	8500A+REL 1	NA 0.55, SOB 90c	22.05	21.9	23.7
	10200A+REL 1	NA 0.55, SOB 90c	22.3	25.3	23.6
	13000A+REL 1	NA 0.55, SOB 90c	21.8	23.4	24.7
Experiment 5	6300A+REL 2	NA 0.55, SOB 100c	0.32	0.35	0.42
	8500A+REL 2	NA 0.55, SOB 100c	0.38	0.43	0.39
	10200A+REL 2	NA 0.55, SOB 100c	0.25	0.31	0.35
	13000A+REL 3	NA 0.55, SOB 100c	0.41	0.45	0.49

4. Conclusion

This entire experiment process to identify the possible solution to eliminate the edge dies defocus issue to improve the overall wafer yield. In this research, the aim is to increase the edge die yield by reducing or eliminating the defocus issue on the wafer edge region by introducing a REL framework. In the experiment's total of five experimental conducted and all the experiments with some significant improvement to overcome the issue. Table 1, shows the entire experiment result. Experiment 1 is the POR data collection for baseline purposes and experiments 2 to 5 with the new approached method to improve the EDD issue. All the collected data from photoresist thickness 6300Å, 8500Å, 10200Å, and 13000 Å is passed without any pattern issue or defocus.

Based on the one-way analysis result Figure 9 shows the difference between edge dis and inner dies. The mean of edge dies is 182.9nm and the mean of inner dies is 183nm. A p-value was calculated for an F-distribution and a p-value of 0.3 was obtained for the above experiment. The p-value of above 0.05 for this case (confidence level is set at 95%), indicating that the null hypothesis is true, the decision is to reject the alternative hypothesis. The comparison data shows the difference between inner dies and edge dies is <1nm. This could be interpreted that experiment five method shows the significant improvement to eliminate the edge die defocus issue. This could also be seen on the t-test circles generated by the one-way analysis of variance (ANOVA) indicating that CD bias for both inner dies and edge dies are comparable. The means for both different combinations were non-distinctive since the circles overlap with one another.

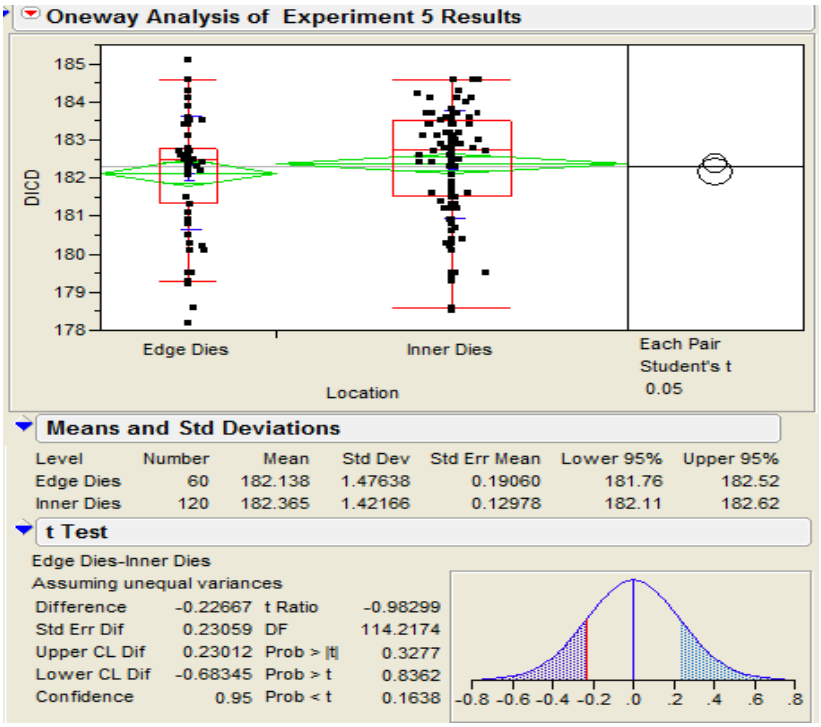

Figure 9: ANOVA - Experiment 5 results

Figure 10 shows the sort yield performance data of stacking maps from 528 wafers with the implementation of the REL method. The mean yield data is showing a significant improvement of yield from 81% (current method) to 94.2% (with the implemented method).

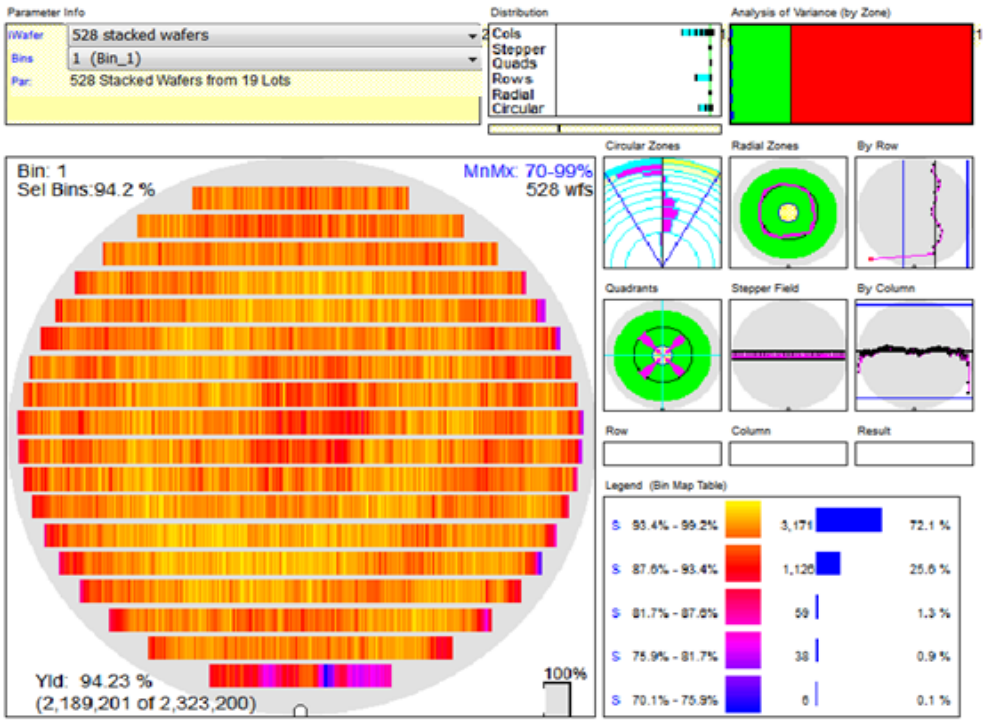

Figure 10: Sort yield performance data with REL method

Figure 11 shows the sort yield data by the zonal area for before and after. The POR condition shows the yield before the implementation is 43.7% at the edge zonal 10 and after the implementation with the REL method, the edge region yield is improved to 84.6%.

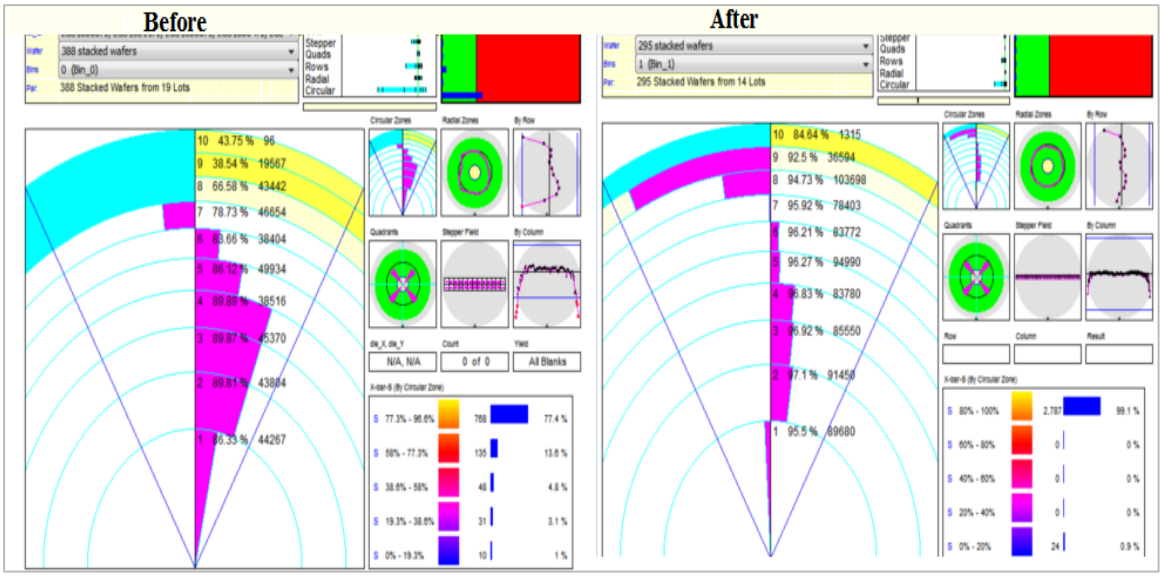

Figure 11: Yield date by Zonal region before and after the implementation

Figure 11 shows the Pareto chart of sort yield data by zonal region for both POR and REL conditions. The REL condition shows the zonal analysis from zonal 8 onwards to zonal 10 is significantly improved.

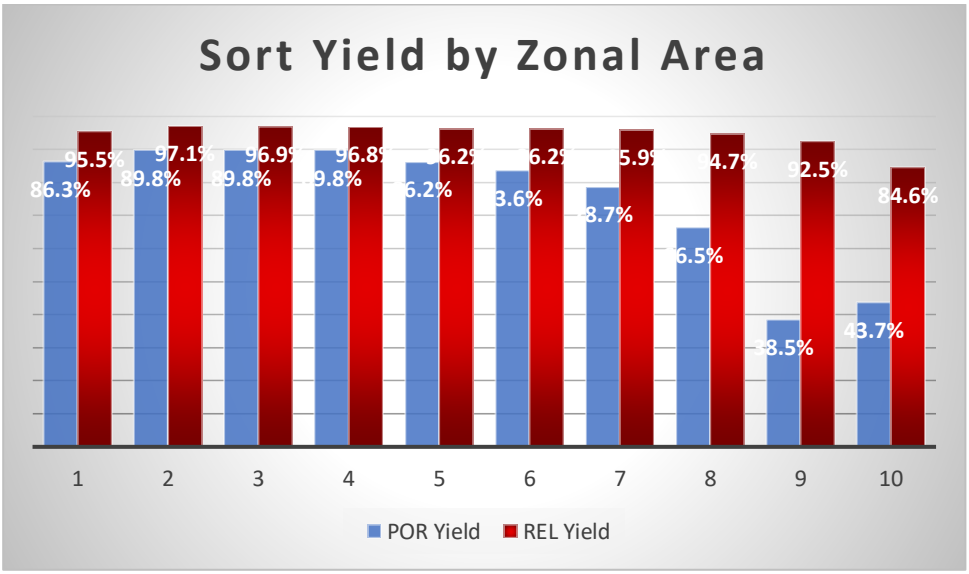

Figure 10: Yield date by Zonal region before and after the implementation

This entire research is using a lithography engineering method and approach to develop a novelty solution is placed to improve the edge die yield defocus issue by applied Radial Exposure Latitude (REL) method for 0.16um technology. Figure 11 shows the sort yield data for three high runner devices from 0.16um technology. The mean of the yield across devices XY01, XY02 & XY03 the gain obtained is at 11.7%. This is a breakthrough achievement by migrating from the POR method to the REL method. In short, the objective has been successfully achieved by implementing a novelty solution with the REL method.

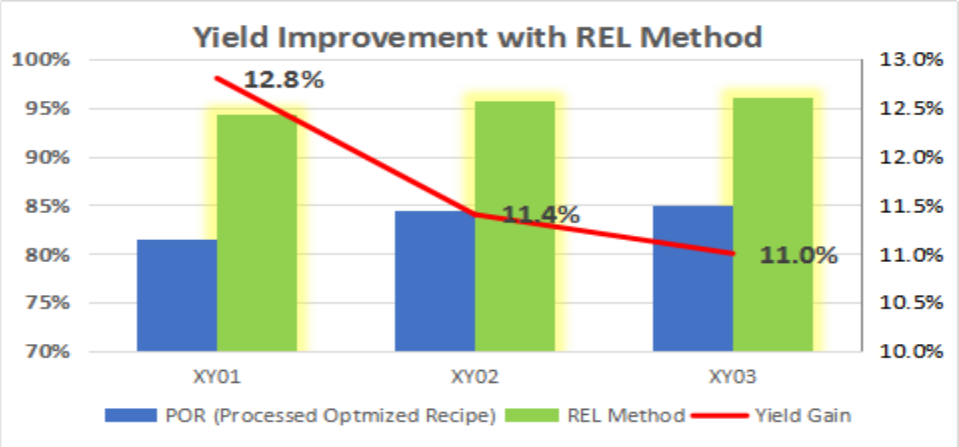

Figure 11: Sort Yield Performance of POR for XY01, XY02 & XY03 Versus REL Method

The purpose of this experiment is to find a novelty solution under the lithography engineering method and approach to improve the edge die yield defocus issue. Based on the yield across devices XY01, XY02 & XY03 the gain obtained is at 11.7%. Initially, with the POR condition, the average yield at the wafer edge dies yield is lower than the center dies yield. The mean of the edge dies is less than 50%. The entire research and analysis identified the edge die defocus issue and novelty solution to improve the edge dies yield and overall sort yield. By applying the REL method, the edge die sort yield is improved from 50% to 85% and the overall yield is improved from 81% to 94%. As this entire research is based on con via layer, as the inter-metal layers using types of resist and thickness, this study can be move on accordingly to implement for pre/post-metal layers in advance technology without any expenditure or cost.

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